METHOD FOR FORMING TWIN BIT CELL FLASH MEMORY
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5   Field of the Invention

[0001]   The present invention relates to a method for manufacturing a flash memory

device, and more particularly to a method of fabricating a nitride read only memory with dual

oxide-nitride-oxide (ONO) gate segments and two bits per cells.

10   Background of the Invention

[0002]   Flash memory devices are used extensively for computer external storage. One

of the goals in manufacturing flash memory is to store a maximum amount of information

using a minimum amount of semiconductor surface area. Another goal of flash memory

fabrication is use of a simple, inexpensive, yet high yield process. Many previous methods

15   for reducing device size add too much complexity and cost. One relatively recent technique

stores two bits in one cell for the purpose for reducing device size. Nitride read only memory

(also called N-bit) cells can be used to accomplish this technique.

[0003]   Fig. 1 illustrates an example prior art Nitride dual bit cell. As illustrated, two

separately chargeable areas 100 and 101 are found within a nitride layer 102 formed in an

20   oxide 103 -nitride-oxide 104 (ONO) sandwich underneath a polysilicon layer 105. However,

some leakage occurs between the first and second bit areas through the Nitride 102. When the

first bit area 100 is charged, electrons leak through nitride 102 to second bit area 101. The

threshold voltage in second bit area 101 can be influenced by the leaked charge, and the data

stored in the second bit could be lost. This problem in dual bit cells is sometimes known as

25   the second bit effect.

[0004]   In view of the drawbacks of the prior method, it is necessary to provide a method that can reduce the cost and complexity in flash memory fabrication and prevent the problem of second bit effect of N-bit memory.

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SUMMARY OF THE INVENTION

[0005]   It is an objective of the present invention to provide a method of fabricating flash memory cells with twin bit cells, and reduce the problem of the second bit effect.

[0006]   It is another object of this invention to reduce the cost and complexity in a fabrication process by self-aligning the buried diffusion implant region and the ONO segment

10   in one process.

[0007]   Roughly described, therefore, in accordance with a preferred embodiment of the present invention, a method is provided for fabricating an N-bit memory device with self-aligned buried diffusion implants and two isolated ONO segments in one cell. The method includes the steps of forming an ONO layer on a substrate, depositing a polysilicon layer,

15   patterning the polysilicon layer, implanting barrier diffusion, trimming the photoresist layer on the polysilicon layer, etching the polysilicon layer by using the trimmed photoresist layer as mask, then removing the photoresist. After removing the photoresist, a nitride layer is filled in the patterned polysilicon layer openings. The etching steps are preformed by using the nitride layer as a mask. The polysilicon layer and part of the ONO layer are removed, and

20   the gate oxide layer is exposed. Two isolated ONO segments are formed by these etching steps. A polysilicon gate is then formed on the gate oxide layer.

[0008]   The embodiment uses photoresist trimming and a polysilicon hardmask method to self-align buried diffusion implant regions and to slice ONO segments. Hence, two ONO segments can be read and be programmed independently to form a twin bit cell

25   structure. The problem of second bit effect of N-bit in the prior art thus can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]   The present invention will be understood and appreciated more fully from the

following detailed description taken in conjunction with the appended drawings in which:

5   [0010]   Fig. 1 is a schematic illustration of a prior art dual bit N-bit cell;

[0011]   Fig. 2 shows a semiconductor substrate including a gate oxide layer, a oxide-

nitride composite layer, a polysilicon layer and a patterned photoresist layer;

[0012]   Fig. 3 shows a result of etching the polysilicon layer;

[0013]   Fig. 4 shows a result of barrier diffusion (BDF) implantation over the structure

10   illustrated in Fig. 3;

[0014]   Fig. 5 shows a result of trimming the photoresist;

[0015]   Fig. 6 shows a result of patterning the polysilicon layer shown in Fig. 5;

[0016]   Fig. 7 shows a result of filling a nitride layer in the opening of the patterned

polysilicon layer;

15   [0017]   Fig. 8 shows a result of removing the polysilicon layer;

[0018]   Fig. 9 shows a result of removing the oxide-nitride composite layer;

[0019]   Fig. 10 shows a result of forming a control gate.

DETAILED DESCRIPTION

20   [0020]   It is to be understood and appreciated that the process steps and structures

described below do not cover a complete process flow for the manufacture of the flash

memory device. The present invention can be practiced in conjunction with various

integrated circuit fabrication techniques that are used in the art, and only so much of the

commonly practiced process steps are described herein as are necessary to support the claims

25   and provide an understanding of the invention.

[0021] Reference is now made to Figs. 2 to 10, which illustrate an embodiment of the fabrication method. In a preferred embodiment of the present invention, the substrate 106 dopant can be either an n-type or a p-type impurity, and is preferably p-type boron with a resistance in the range of 8 to 12 O/cm^2. In this preferred embodiment, a p-type boron

5   impurity is used. Next, a dielectric layer 107, which is used as a thin tunnel layer and is preferably an oxide layer, is grown over the substrate typically to a thickness of between 40Å and 200Å by a conventional dry oxidation method. A typical oxidation temperature is about 800°C, but it can vary between 750-1000 °C. A preferred thickness of the dielectric layer is 50Å. Then an insulating composite layer 108, which is preferably a nitride layer 109

10   underlying an oxide layer 110, is formed over the semiconductor substrate 106. The nitride layer 109 thickness is in the range of 40Å to 200Å with a preferred thickness of 70Å. The top oxide layer 110 is preferably formed of a thickness about 60Å to 120Å. Then a first sacrificial layer 111, which is preferably a polysilicon layer, is formed on the surface of the composite layer 108. Low-pressure chemical vapor deposition (LPCVD) is used to deposit

15   this doped polysilicon layer or doped amorphous silicon layer with a thickness of 200Å to 3000Å. In this preferred embodiment, the first sacrificial layer is 1200Å thick. Then a protective patterning layer 112, which is preferably a photoresist layer, is formed on the surface of the first sacrificial layer 111 and patterned.

[0022] Referring to Fig. 3, the first sacrificial layer 111 is etched with the patterned

20   protective patterning layer 112 as mask. The etching process is preferably a dry etching process, for example a RIE plasma etching process with chlorine (Cl$_2$), hydrogen bromide (HBr) and oxygen (O$_2$) plasma.

[0023] Referring to Fig. 4, the buried diffusion implant (BDF) regions 113 are formed in the semiconductor substrate 106 by implanting ions over the structure illustrated in Fig. 3.

25   The ions can be either n-type or p-type impurities 114 implanted with energies in the range of

about 20 to about 150 KeV, and a dosage in the range of about 0.5×10^{14} to about 2×10^{18} atoms/cm^2. The ion impurity is preferably Arsine in this preferred embodiment. It will be appreciated that this is a self-aligned implant in which the bit lines are self-aligned to the substrate 106.

5   **[0024]**   Referring to Fig. 5, the protective patterning layer 112 is trimmed by using a conventional etching process, and preferably a dry etching process. The dry etching process gases include Fluorine-based gas, carbon monoxide (CO) and O_2 plasma. In this preferred embodiment, the process gases are CF_4 and O_2.

[0025]   As shown in Fig. 6, the first sacrificial layer 111 is etched by using the

10   protective patterning layer 112 illustrated in Fig. 5 as mask. The etching process is preferably a dry etching process, for example, a RIE plasma etching process with Cl_2, HBr and O_2 plasma.

[0026]   Referring to Fig. 7, a second sacrificial layer 115 is filled in the openings 116 illustrated in Fig. 6. The second sacrificial layer is preferably a silicon nitride layer formed by

15   a conventional CVD process, and preferably a LPCVD process. The precursors of the low pressure chemical vapor deposition process are dichlorosilane (SiCl$_2$H$_2$), silane (SiH$_4$) and ammonia (NH$_3$).

[0027]   As Fig. 8 shows, the first sacrificial layer 111 is removed by using a conventional etching process. The etching process is preferably a dry etching process that use

20   Cl_2, HBr and O_2 plasma.

[0028]   Referring to Fig. 9, the insulating composite layer 108 is removed by using the second sacrificial layer 115 illustrated in Fig. 8 as mask, thereby exposing the dielectric layer 107. Preferably dry etching is used in this step, with different etching selectivity between the composite layer 108 and the tunnel oxide layer 107. Materials such as CHF_3, CF_4, HBr and

25   SF_6 can be used. It is acceptable if some amount of the tunnel oxide layer 107 is also

removed in this step, as long as the amount is controlled. Importantly, it can be seen that isolated ONO segments are formed by self-aligned etching of the insulating composite layer without using any photolithographic process.

[0029]   As shown in Fig. 10, the second sacrificial layer 115 is removed by using a

5   conventional etching process and a control gate 117 is formed. The control gate is preferably a polysilicon gate.

[0030]   As used herein, the terms "above" and "below" are intended to be interpreted relative to the substrate as a base. Similar interpretations are intended for the words "overlying", "underlying" and "superposing". In addition, as used herein, a "layer" can

10   include "sub-layers", each of which can itself also be considered herein to constitute a "layer".

[0031]   Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is to be understood that the present invention is capable of use in various other combinations and

15   environments and is capable of changes or modification within the scope of the inventive concept as expressed herein.